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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,661	07/31/2001	Praveen K. Parvathala	219.39515X00	1090

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EXAMINER
TABONE JR, JOHN J

ART UNIT	PAPER NUMBER
2133	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,661	PARVATHALA ET AL.	
	Examiner	Art Unit	
	John J Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 11, 21, 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

This claim recites the limitation "converting FRIT kernel into kernel test patterns". It is not clear how a FRIT kernel is converted into kernel test patterns and, therefore, renders the claim indefinite. Further clarification is required.

Claims 2-10:

These claims are rejected because they depend on claim 1 and contain the same problems of indefiniteness.

Claims 11and 21:

These claims recite the limitation "receiving the FRIT kernel into kernel test patterns". It is not clear how a FRIT kernel is received into kernel test patterns and, therefore, renders the claim indefinite. Further clarification is required.

Claims 12-20 and 22-30:

These claims are rejected because they depend on claims 11 and 21, respectively and contain the same problems of indefiniteness.

Claim 31:

These claims recite the limitation "...to store a FRIT kernel in kernel test patterns". It is not clear how a FRIT kernel is stored in kernel test patterns and, therefore, renders the claim indefinite. Further clarification is required.

Claims 32-38:

These claims are rejected because they depend on claims 31 and contain the same problems of indefiniteness.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6, 11-14, 16, 21-24, 26, and 31-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Williams et al. (US-2002/0093356).

Claims 1, 11, 21 and 31:

Williams teaches the ATPG tool 12 is generally described as a computer system that is programmed to execute ATPG processes (FRIT kernel) whose primary purpose is to efficiently generate test vectors (kernel test patterns). Williams further teaches the ATPG tool 12 writes the test patterns into a first memory (memory1) of tester 14 (tester memory). (Page 3-4, ¶ 33-35). Williams discloses the tester 14 scans test vectors

(loading kernel test patterns) into memory cells of the DUT 16 (on-board memory) during test mode and the DUT 16 is then operated (executing functional test) which generates a set of outputs. Williams further discloses that the tester 14 applies the test patterns to the DUT 16 and examines the real output of the DUT 16 against the expected output (comparing test results with an expected test result). The tester 16 then recalls the output from the DUT 16. The test vectors provide the necessary inputs in order to detect the presence of faults within the DUT 16 (check for manufacturing faults). (Page 4, ¶ 34).

Claims 2, 12, 22, 32 and 33:

Williams teaches the ATPG tool 12 (FRIT kernel/SBE) contains a netlist description 18 of the electronic design that is found within the DUT 16 and can be written in HDL (high level design language) (computer model). Williams further teaches the ATPG tool 12 not only generates test patterns, but during simulation it also captures the expected outputs of the netlist 18 (expected test result obtained from computer modeling) based on the application of these test patterns. (Page 3-4, ¶ 33).

Claims 3, 13 and 23:

These claims have the same limitation as claims 2, 12, 22 above and are rejected per those claims.

Claims 4, 14, 24 and 34:

Williams teaches that program instructions (machine code) executed by the ATPG system can be stored in RAM 102, ROM 103, or the storage device 104. Williams also teaches a central processor 101 (test program execution module) coupled with

bus 100 for processing information and instructions. (Page 6, ¶ 52, 53). Williams also discloses the LFSR circuit 230 will generate a reproducible sequence of pseudo random bits and acts like a pre-specified compressed data repository for the random bits of the test pattern (compressed test results). Williams further discloses that testing circuitry, like the LFSR 230, can be incorporated on the DUT 16. (Page 4,5, ¶ 38, 43, 46).

Claims 6, 16 and 26:

Williams teaches the DUT 16 is typically an integrated circuit or "chip." A microprocessor is a type of integrated circuit. (Page 3, ¶ 33).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7, 8, 17, 18, 27, 28 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US-2002/0093356).

Claims 7, 17, 27 and 36:

Williams teaches the ATPG tool 12 generates a set of test patterns that are used to locate faults within the DUT 16 (generate test sequences). Williams further discloses that the tester 14 applies the test patterns to the DUT 16 (runs the test sequences) and examines the real output of the DUT 16 against the expected output (comparing test results with an expected test result). The tester 16 then recalls the output from the DUT

16. The test vectors provide the necessary inputs in order to detect the presence of faults within the DUT 16 (check for manufacturing faults). (Page 4, ¶ 34). Williams does not explicitly teach that the microprocessor performs these steps, however, Williams does suggest that testing circuitry, like the LFSR 230, can be incorporated on the DUT 16. (Page 5, ¶ 46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to move the test sequence generation and execution functions to the DUT 16. The artisan would be motivated to do so because this would reduce the throughput of data flowing from the tester to the DUT 16.

Claims 8, 18 and 28:

These claims have the same limitation as claims 2, 12, 22 above and are rejected per those claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 9, 10, 15, 19, 20, 25, 29, 30, 35, 37, and 38 rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US-2002/0093356) in view of Gittinger et al. (US-5668815).

Claims 5, 15, 25 and 35:

Williams does not explicitly teach an exception handler to handling illegal conditions such as infinite loops, however, Williams does teach that program instructions can be stored in the RAM 102, ROM 103, or the storage device 104. (Page 6, ¶ 54). Gittinger teaches a "watchdog timer" (exception handler) is initialized by a software instruction just prior to performing an instruction or instructions which may result in an infinite hang condition (e.g. infinite loop, an instruction which never completes executing because data is never returned from an external device, etc.). (See col. 7, lines 31-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the software in Williams' ATPG system 12 to include Gittinger's "watchdog timer". The artisan would be motivated to do so because it would allow Williams to provide an interrupt that would cause the processor to exit from the instruction code that is experiencing the infinite hang condition.

Claims 9, 19, 29 and 37:

Williams does not explicitly teach generating a number of instruction sequences, however, Williams does teach that program instructions can be stored in the RAM 102, ROM 103, or the storage device 104. (Page 6, ¶ 54). Gittinger suggests instructions that may be performed by tester 42 for looping multiple passes of selected test patterns for microcontroller 10 depicted in FIG. 8. The code may be extended to perform passes for all selected patterns by storing the patterns in memory and using a counter to select the patterns and loop through the code a number of times equal to the number of selected patterns. (See col. 18, lines 11-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Gittinger's looping instructions for

testing a combination of multiple passes through number of selected test patterns can be programmed into Williams' program instructions in the RAM 102, ROM 103, or the storage device 104. The artisan would be motivated to do so because this would add flexibility to test multiple patterns successively and increase the testability of the micrproceesor.

Claims 10, 20, 30 and 38:

Williams teaches the MISR generates a signature value (generates signatures). Williams also teaches the ATPG tool (SPE) can simulate the expected resultant signature, and this value is stored in memory 545. Therefore, circuit 540 can compare the expected final signature against the actual final signature as stored in signature latch 535. If there are any errors or mismatches, the error flag 550 is set. If the error flag 550 is ever set, then verification for the DUT fails (test sequence is good or bad). (Page 7, ¶ 563).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Vigil et al. (US-5,732,209)

Vigil teaches a test program executed bye CPU cores. Loading the test program from a tester to an on-chip memory (ROM) to store the test program. The ROM contains test routines to test cache memory. The invention also creates compares signatures. Tests for good/bad chip. Compress signatures. Apply to claims 1, 7, 11, 21 and 31.

Le et al. (US-6,578,169)

Le teaches a semiconductor test system to evaluate a device under test (DUT) which is typically a memory IC such as a RAM and a flash memory, a logic IC such as a microprocessor and a DSP , or a system IC such as a system-on-a-chip. Le teaches loading a test program and various test conditions, a patterns memory, data failure memory, an event controller for producing test signals, and a pattern comparator. Apply to claims 1, 6, 11, 21 and 31.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJT

Albert DeCady
Primary Examiner